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MICRO 800 SERIES MINI COMPUTERS

Literature Request Card

BROCHURES

- ☐ MICRO 800/810 Mini Computers
- ☐ MICRO 812 Communications/Processor

REFERENCE MANUALS

- ☐ MICRO 800
- ☐ MICRO 810
- ☐ MICRO 812

PROGRAMMING MANUALS

- ☐ AP800 Assembly Program
- ☐ AP810 Assembly Program
- ☐ SIM800 Simulator
- ☐ MAP810 Assembly Program, Teletype Operating System & Tape Editor Program
- ☐ MAP810 Firmware Manual

TECHNICAL NOTE

- ☐ Introduction to Microprogramming

INTERFACE DATA

- ☐ 800/810 Interface Manual
- ☐ Central Processor Option Board (8400)
- ☐ Input/Output Line Driver and Receiver Board (8700)
- ☐ Parallel Teletype Controller (8701)
- ☐ General Purpose I/O Board—Wire Wrap (8702)
- ☐ Priority Interrupt Board (8703)
- ☐ Direct Memory Access Selector Channel (8704)
- ☐ Input/Output Expander—32 bits (8705)
- ☐ Synchronous Modem Controller (8801)
- ☐ Multiple, Low-Speed Modem Interface (8803)
- ☐ Multiple, Teletype Interface
- ☐ Card Reader Interface (8907)
- ☐ Paper Tape Reader/Punch (8908)
- ☐ Rotating Memory System Controller (8902)

Additional data required: _____

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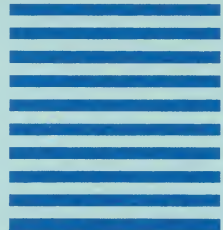
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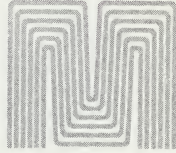
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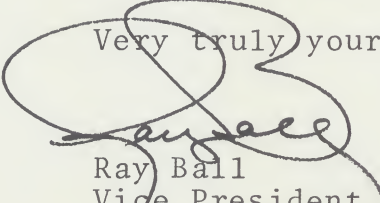
for your interest in the MICRO 800 Series Computers. We are enclosing technical data and an informative Technical Note entitled, "Introduction to Microprogramming."

The MICRO 800 Computers provide the best value in the industry for dedicated system applications. Furthermore, Micro Systems Inc. offers engineering and microprogramming services for the computer. This means that a configuration meeting your specific functional requirements can be provided with less hardware cost than conventional systems. Programming and special interface control in the MICRO 800 Series are also less expensive. The maximum I/O transfer rate far exceeds that of other computers in the same price classification.

The minimum system with a central processor, 15 general purpose hardware registers, power supply, 19-inch rack mountable chassis and a basic control console sells for only \$2,550. Up to 1,024 words of read only memory, 16,000 bytes of high-speed magnetic core memory, and 5 interface boards can be added to the standard MICRO 800 system. The MICRO 810, a microprogrammed, general purpose computer, has a base price of \$6,530 which includes a 4K X 9 core memory. The MICRO 812, our Data Communications Processor, is priced from \$10,890. Most MICRO 800, 810, or 812 configurations can be delivered in less than 30 days, and attractive O.E.M. discounts are available.

For additional specification or pricing data on the MICRO 800 Series Computers, please contact your Micro Systems Inc. sales engineer. His business card is attached.

Very truly yours,


Ray Ball
Vice President, Marketing

/jt

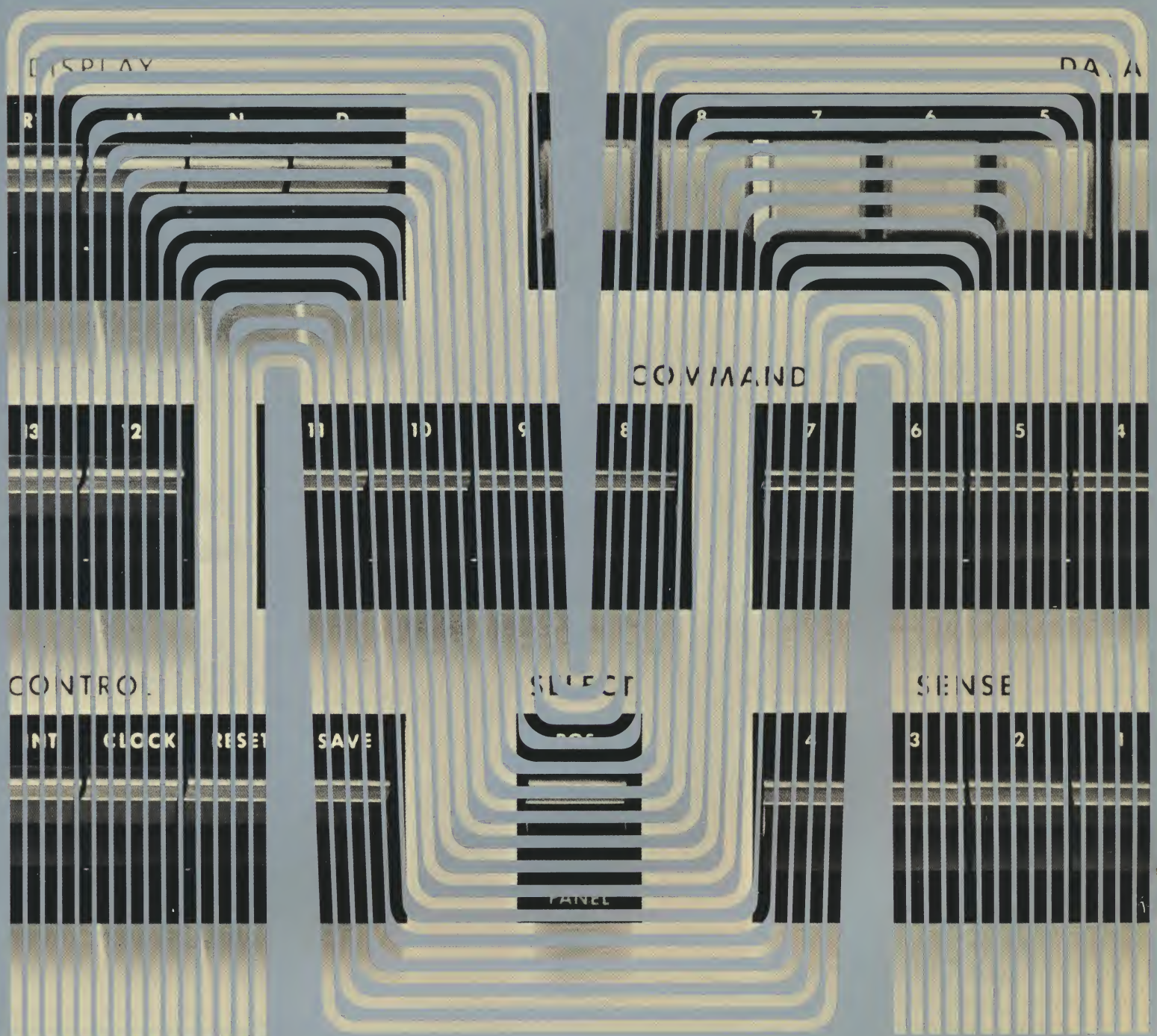
A Microdata Subsidiary

MicroSystems



Francis T. Lynch
District Sales Manager

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Phoenixville, Pennsylvania
19460
Telephone (215) 933-0036



The Micro 800 Series Computers

A Mini-seminar

Q. Who is Micro Systems Inc.?

A. Micro Systems Inc. is a company that has become a leading manufacturer of small computers in a relatively short time. We have accomplished this by staffing ourselves with the best talent available in all phases of computer technology; both computer system generalists as well as specialists in core memories, read only memories, discrete and integrated circuitry, programming, software support, and application engineering. In the manufacturing area, we established a high volume capacity in advance of soliciting customer orders to meet the dependable delivery needed by volume OEM users of small computers. In our first year of operation we more than doubled our manufacturing plant space, and we will more than double it again during the next year.

Q. Why do we need another manufacturer of small computers?

A. Very simple; our new MICRO 800 and 810 Computers can save OEM users substantial amounts of money because all but the essential hardware needed for a dedicated application has been stripped away. Flexibility and versatility, though, have not been sacrificed due to unique organization and proprietary micro-programming techniques. Functional modularity permits the systems to be expanded or reduced to the exact configurations needed for specific applications — again saving the user money. The core memory is expandable to 32,768 bytes of 8, 9, or 10 bits. (Certain applications for the MICRO

800 Series may require no core memory.) 16K bytes can be accommodated in the basic enclosure.

Read only storage can be expanded to 1,024 words in modules of 256 words. All system modules, including custom interfaces, are pluggable for ease of maintenance and expandability.

Both standard and special system interfaces are also mounted within the basic enclosure. Input/output cabling is simple and inexpensive, and various types of control consoles are pluggable and interchangeable.

Q. What's the difference between the MICRO 800 and 810 Computers?

A. The MICRO 800 is a high speed, micro-programmable digital computer. It provides a medium where the user can define his own instructions, input/output, and interrupt capabilities to suit his particular needs. The MICRO 800 provides a degree of flexibility and speed which cannot be obtained in conventional computers with fixed instruction sets and core memory programs. The MICRO 800 executes programs located in a read only store with a command execution time of 220 nanoseconds.

The MICRO 810 is a microprogrammed adaptation of the MICRO 800 System. The microprogram (firmware) converts the basic MICRO 800 System into a software programmable, macro level general purpose computer. The MICRO 810 contains 16-bit registers, variable precision operations, and 89 instructions including multiply and divide.

MICRO 810 programs are stored in the core memory and their instructions are interpreted by microprogram sub-routines residing in the read only store.

Q. Is other firmware available?

A. Other specialized microprograms (firmware) are being continually developed by Micro Systems Inc. and these are available for customer use. In addition, MSI will be pleased to assist in the development of proprietary firmware for users of the MICRO 800 Series.

Q. Where can these computers be used?

A. The MICRO 800 and 810 are well suited for a variety of OEM applications because of their high speed, microprogramming flexibility, functional modularity, and system-oriented packaging. Typical application areas include process control, data communications, data acquisition, test automation, and numerical control. The computers can also be used as pre-processor batch terminal controllers, and peripheral controllers for card readers, card punches, visual displays, line printers, magnetic tapes, or almost anywhere an electronic controller/computer is needed.

Q. What makes the MICRO 800 Series Computers so versatile?

A. The MICRO 800 Series Computers are versatile because they can be used in several ways. Where maximum throughput is required, the application can be programmed directly with the microcommand. While the read only store cannot be

electrically altered, variable control parameters can reside in the core memory. Where flexibility and ease of programming are desired and maximum throughput is not required, the MICRO 810 with its macro level instruction set is used.

Emulation of other general purpose computers can be microprogrammed so as to protect investment in application software or to provide a proprietary instruction set.

Special purpose computers can be created by appropriate microprogramming for such tasks as data compressors, telemetry decommutators, and signal processors.

Q. Is software available?

A. A wide range of software is available for the MICRO 800 Series Systems and the library is being expanded continually.

Present software includes SIM 800, a MICRO 810 program to simulate the MICRO 800 computer logic; AP800 and AP810 FORTRAN IV cross assembler programs; teletype operating system, two pass assembler, and tape editor for the MICRO 810; and software and firmware processor and memory diagnostics.

Q. What are the prices of the MICRO 800 and 810?

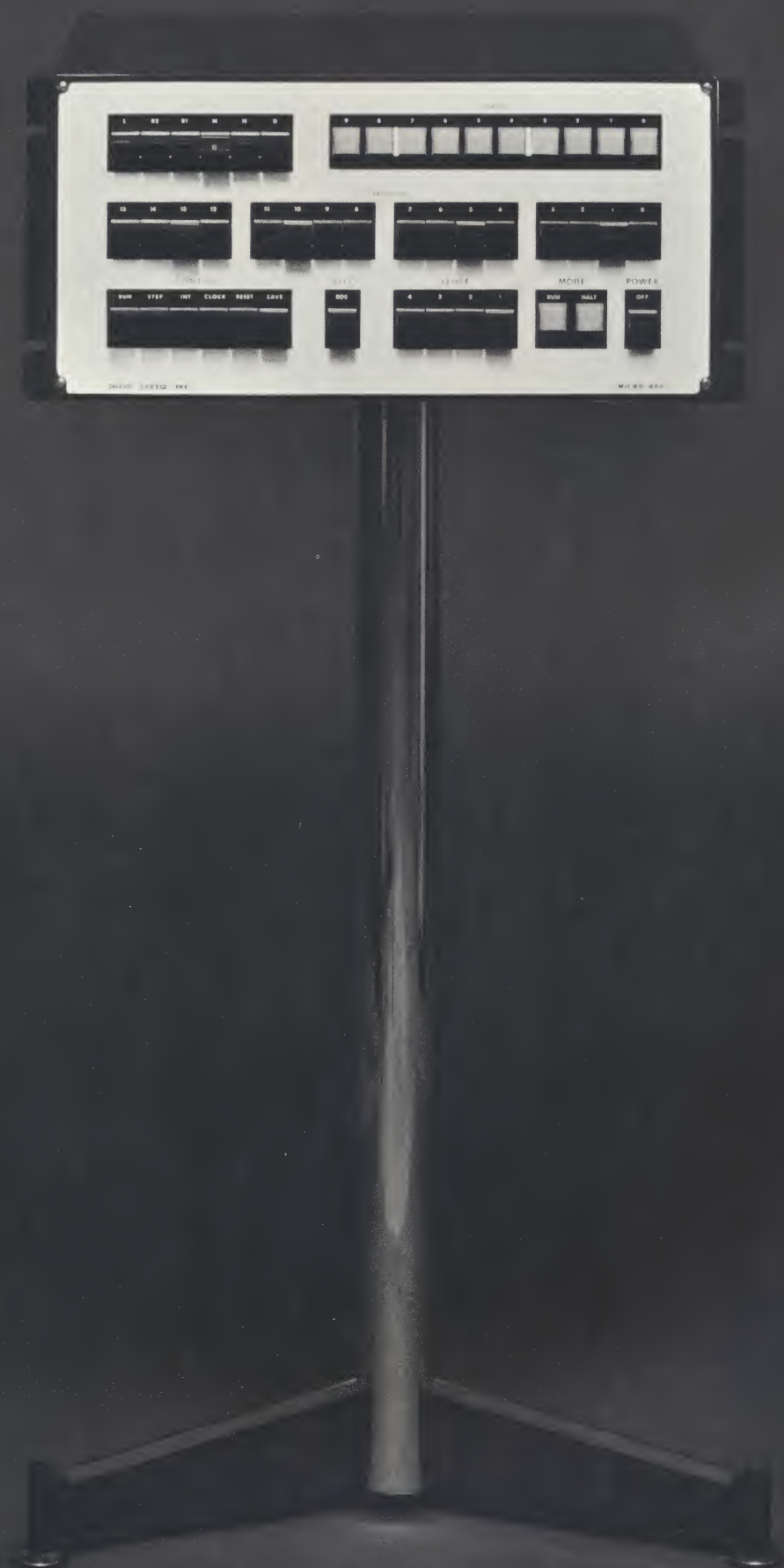
A. The basic price of the MICRO 800 is \$3,200 (with quantity discounts to 40 percent). This includes a basic processor containing 16 multipurpose registers, 256 words of read only

store, basic console, enclosure, and power supply to function as a micro-programmed controller. Up to 32K bytes of core memory, direct memory access, power fail and auto-restart, and many standard or special options can be added to fit a broad spectrum of system requirements.

The basic price of the MICRO 810 is \$6,900, which comprises a MICRO 800 system with 768 words of read only store, a 4,096 word x 8 bit core memory, and teletype interface.

Q. What about delivery?

A. As we said, we have geared our production schedules to keep ahead of user demand. As a result, we began building 800's before we began selling them, and we're now in volume production. We are offering 30-day or sooner delivery. Large-scale orders or specially designed systems take a little longer.



The Micro 800

General Description

The MICRO 800 is a very unusual small computer. Its high speed, microprogramming flexibility, functional modularity, and system oriented packaging make it ideally suited for dedicated volume OEM applications.

The MICRO 800 not only forms the hardware nucleus of other MSI computers, such as the Model 810, but it may be applied as a low-cost solution by users to specific digital applications. The MICRO 800 can also be used to create other higher level computers whose architecture and instruction set are tailored to the user's application.

Sequences of command steps which make up a MICRO 800 program are commonly referred to as "firmware" since they are placed into a Read Only Storage (ROS) consisting of a matrix of discrete diodes. Commands read out of the ROS every 220 nanoseconds exert a powerful micro control over the computer's logic. Printed circuit board ROS modules of 256 16-bit words may be used-up to a maximum of 1024 words.

This microprogram firmware capability, combined with other proprietary design features, gives the MICRO 800 features which are unmatched by any other computer presently on the market.

For example, the computer can be used without a core memory as an inexpensive controller or data concentrator. When memory is required for storage of variable parameters, tables, or data, high-speed core memory may be added to the system. The MICRO 800 can also be microprogrammed to emulate other general or special purpose computers enabling

the software of these machines to be compatible with the MICRO 800. In such a case, additional interface hardware can be furnished to provide plug-to-plug compatibility with other computers. As for speed, the 1.1 microsecond core memory cycle time and 220 nanosecond command execution time make the MICRO 800 the fastest machine in its class.

The functional modularity of the MICRO 800 permits the system to be expanded or reduced to the exact configuration needed for any application. The core memory is expandable from 0 to 32,768 bytes (8, 9, or 10 bits) in 4,096 byte increments. A 1,024 byte core memory is also available for small, inexpensive systems. Main frame options including memory parity, power fail/automatic restart, real time clock, and input/output interfaces, are implemented on card modules which plug into the basic MICRO 800 enclosure.

In addition to low unit cost, the MICRO 800 system can also reduce overall system cost. The high speed execution of firmware routines allows the processor logic to be time shared so as to minimize input/output interface hardware. An example of this technique would be serial teletype input/output which involves character assembly and disassembly.

The microprogramming concept provides exceptionally high performance with an unusually small amount of internal hardware. This enhances system reliability and reduces maintenance requirements. The basic computer consists of two identical data boards, each of which is a 4-bit slice of the computer's data paths and registers, and a single

control board which provides command decoding and timing. All standard processor options are contained on a single printed circuit board.

Another outstanding feature of the MICRO 800 is the use of available card slots in the basic enclosure for interfaces and device controllers. Four card slots are dedicated for this purpose along with unused ROS slots. A card slot is reserved for the Direct Memory Access channel and a second DMA channel may be inserted in one of the core memory card slots. The power supply has ample capacity to power a fully expanded version of the MICRO 800. These features can yield significant cost savings through the elimination of costly expansion cabinets, power supplies, cables, and logic.

The Micro 800 Specifications

Type

A high speed, byte oriented, microprogram-mable computer designed for dedicated applications.

Arithmetic

Parallel, binary, fixed point, one's and two's complement for negative numbers.

Commands

Fifteen basic commands including add, subtract, copy, OR, exclusive OR, AND, read/write memory, I/O control, load file, load register, add to file, and skips on arithmetic and logical tests.

Speed

Clock rate is 4.55 MHz. All instructions are executed in 220 nanoseconds except for the jump and skip commands, when the skip is taken, which require an additional 220 nanoseconds interval.

Core Memory

Memory modules of 4,096 bytes by 8, 9, or 10 bits and 1,024 bytes by 9 bits are available. The memories use wide temperature range lithium cores and operate at 1.1 microseconds full cycle and 0.66 microsecond half cycle times. Memory is field expandable to a maximum of 32,768 bytes. Extra memory bits may be used for memory parity and/or special applications.

Read Only Storage

Read Only Storage (ROS) uses discrete diodes in printed circuit board modules of 256 16-bit words. ROS cycle time is 220 nanoseconds.

Input/Output

An 8-bit parallel byte I/O bus permits programmed and fully automatic concurrent transfers. A serial I/O interface allows interfacing teletypes or similar devices. A Direct Memory Access (DMA) channel has a maximum transfer rate of 909,000 bytes per second.

Interrupts

An interrupt request flag, which can be tested by microcommands, is available. I/O interfaces are designed for generating priority interrupts.

Logic

TTL logic elements including an extensive amount of MSI types, packaged in DIP ceramic packages, are used. DTL circuitry is used for I/O interfaces.

Cabinet

The processor, memory to 16K, I/O interfaces, power supply, and fan are enclosed in a cabinet measuring 8-3/4" high, 17-3/5" wide, and 23" deep. Fully expanded cabinet weight is 75 pounds.

Panels

The *system control panel* permits display of all registers, manual command execution, and control switches. The *operator's panel* is the same as the system panel but displays only the file registers. The *basic control panel* provides only the basic control switches.

Power

115/230VAC $\pm 10\%$, 47-63 cycles, 340 watts AC.

Environment

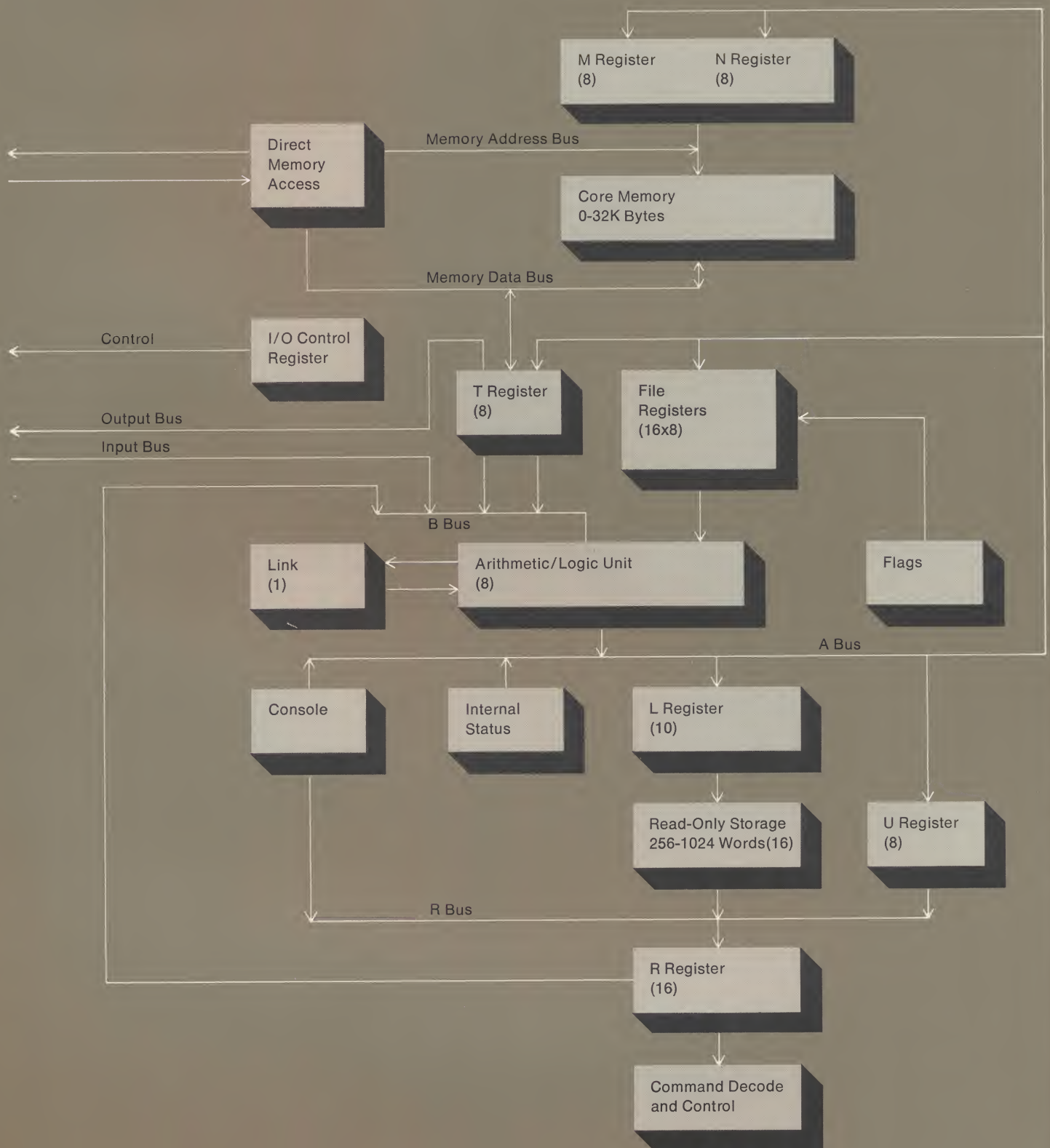
0-50°C (32°-122°F), 10-90% humidity (without condensation).

Software

AP800 is an assembly program for generating the Read Only Storage diode maps, which is written in FORTRAN IV. A simulator which runs on the MICRO 810 provides for interactive simulation of firmware programs.

Micro 800

Block Diagram



Micro 800

Functional Organization

The MICRO 800 processor is organized around an 8-bit arithmetic/logic unit (ALU) which performs all arithmetic, logic, and shifting functions. One of the inputs to the ALU is a file of registers containing 15 general purpose registers and one register of internal and external condition flags. The other input to the ALU is the B bus which derives its input from the true or complement output of the temporary buffer (T register), the input bus, or an eight-bit literal contained in the command. The type of command, selection bits in command, and the state of the I/O control register determine the B bus input which may be zero or all one bits. The output of the ALU is the input to the file registers and other machine registers.

The read only storage is organized into 256 word modules. Each of the modules (four maximum) receives an address from the machine's program counter (L register) which contains the read only storage address of the next command to be executed. The output of the ROS is gated onto the R bus which is then clocked into the 16-bit command register (R) where the command is decoded. The U register is allowed to OR onto the eight high order bits of the R bus under certain conditions to allow for dynamic modification of the ROS program steps. The control console command switches may be entered onto the R bus, instead of the read only storage modules, to provide for manual control of the commands.

The core memory consists of 4096 byte modules with expansion to a maximum of 32,768 bytes. Special applications may eliminate the need for core memory and use only the read only store and file. Data transfers between

the core memory modules and the processor's T registers or the Direct Memory Access (DMA) module are performed over the bi-directional memory data bus. The memory address bus provides the memory address from the processor's memory address register (M and N) or the DMA module.

Input/output is performed by an eight-bit input bus, an eight bit output bus (which originates with the T register), and a group of control lines which are under microprogram control through the I/O control registers.

The Micro 810

General Description

The MICRO 810 is a general purpose computer which is a microprogrammed adaptation of the MICRO 800. Microprogrammed subroutines, configured in the ROS, interpret macro instructions of programs stored in the core memory.

The MICRO 810 provides the user with a powerful macro level programmed computer but retains all the modular and functional advantages of the MICRO 800. The MICRO 810 allows for considerably larger programs than are possible with the 800 combined with ease of programming and program flexibility. Some of the advantages of the MICRO 800 can be obtained by adding additional problem oriented macro instructions or firmware subroutines to the MICRO 810.

The Model 810 makes use of less than 768 words of ROS to provide the following functions:

Variable Word Length (8, 16, 24, or 32 bit arithmetic load and store instructions)

Eight Operand Addressing Modes

Four 16-bit Operational Registers (A, B, X, P)

A Repertoire of 89 Powerful Instructions including: 17 control instructions, 16 conditional jumps, 12 shifts, 8 input/output instructions, 16 register operate instructions, 18 memory referencing instructions, multiply and divide

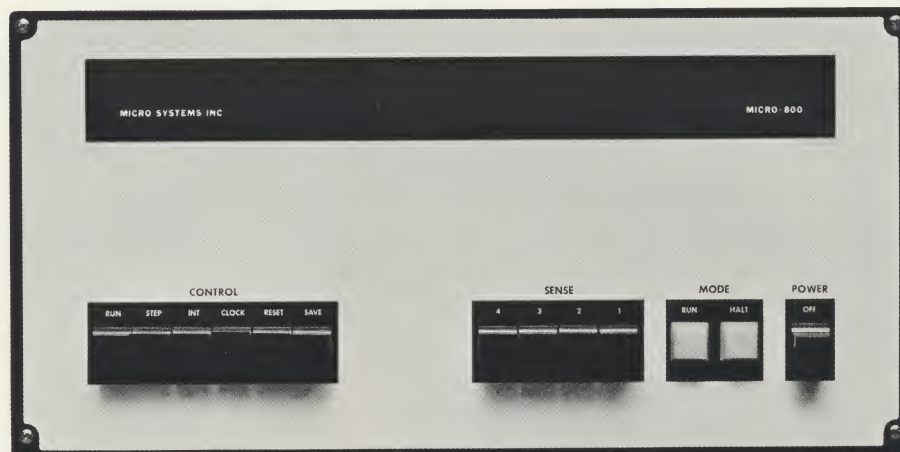
Four types of Input and Output: programmed with A register, B register, or memory; concurrent; serial teletype; and DMA

Priority Interrupt with up to 64 individual interrupt lines

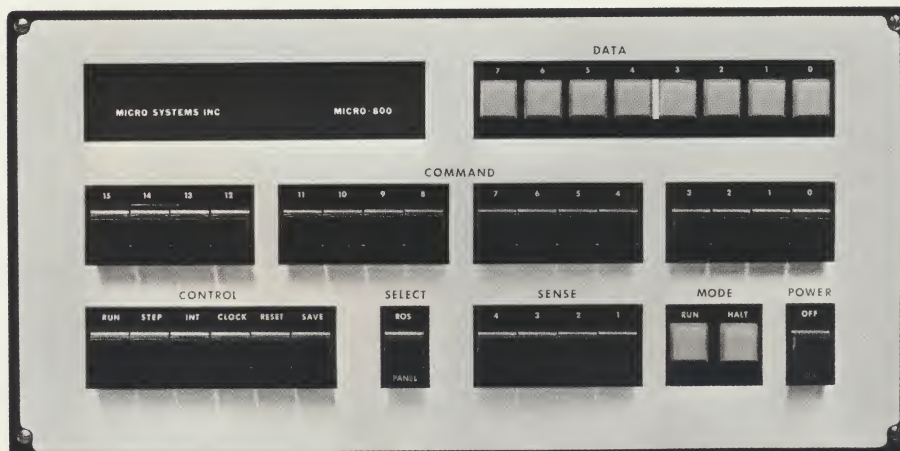
Processor Options including memory parity, power fail/automatic restart, and real time clock

Boot-strap Loader

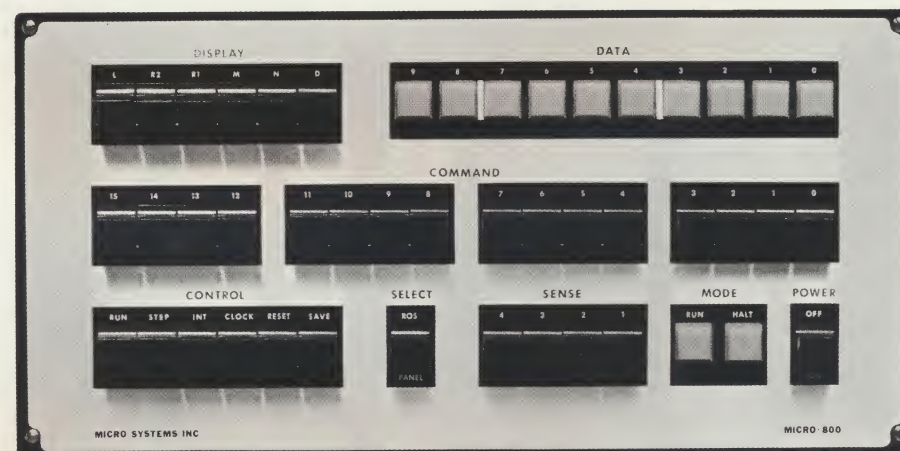
Basic Control Panel



Operator Control Panel



System Control Panel



Micro 810

Specifications

Type

A microprogrammed general purpose computer designed for dedicated applications.

Word Length

Memory is byte addressable, registers are 16 bits in length, and arithmetic operations are 8, 16, 24, or 32 bits in length.

Arithmetic

Multi-precision, parallel, binary, fixed-point, two's complement.

Addressing

Eight addressing modes including relative, index, indirect, and literal.

Registers

Six operational registers:

A Register

Accumulator

B Register

Auxiliary accumulator for low order 16 bits of 24 and 32-bit data

X Register

Index register

P Register

Program counter

W Register

2-bit word length mode register

O Register

1-bit overflow flag

Core Memory

Memory modules of 4,096 bytes by 8, 9, or 10 bits and 1,024 bytes by 9 bits are available. The memories operate at 1.1 microseconds full cycle time and 0.66 microsecond half cycle time. Memory is field expandable to a maximum of 32,768 bytes. Extra memory bits may be used for memory parity and special applications.

Read Only Storage

Read Only Storage (ROS) uses discrete diodes in printed circuit board modules of 256 16-bit words. ROS cycle time is 220 nanoseconds.

Input/Output

An 8-bit parallel byte I/O bus permits programmed and fully automatic concurrent transfers. A serial I/O interface allows interfacing teletypes and other similar devices. A Direct Memory Access (DMA) channel has a maximum transfer rate of 909,000 bytes per second.

Interrupts

A priority interrupt system allows internal interrupts on power failure, real time clock, memory parity error, and external interrupts on the byte I/O bus. An optional board provides for eight programmable external interrupts.

Logic

TTL logic elements including an extensive amount of MSI types packaged in DIP ceramic packages are used. DTL circuitry is used for I/O interfaces.

Cabinet

The processor, memory to 16K, I/O interface, power supply, and fan are enclosed in a cabinet measuring 8-3/4" high, 17-3/5" wide, and 23" deep. Fully expanded cabinet weight is 75 pounds.

Panels

The *system control panel* permits display of all registers, manual command execution, and computer control switches. The *operator's panel* is the same as the system panel but displays only the file registers. The *basic control panel* provides only computer control switches.

Power

115/230VAC $\pm$ 10%, 47-63 cycles, 340 watts AC.

Environment

0-50°C (32°-122°F), 10-90% humidity (without condensation).

Software

Software for the MICRO 810 includes AP810, a FORTRAN IV written assembly program, a teletype operating system (TOS), two-pass assembly program, tape editor and diagnostic programs.

Micro 810

Instructions

Operation Code	Mnemonic	Instruction Name
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Control

00	HLT	Halt
01	TRP	Trap
02	ESW	Enter Sense Switches
03	PMP	Protect Memory Page
04	DIN	Disable Interrupt System
05	EIN	Enable Interrupt System
06	DRT	Disable Real Time Clock
07	ERT	Enable Real Time Clock
08	RO1	Reset Overflow and Set Word Length to 1
09	RO2	Reset Overflow and Set Word Length to 2
0A	RO3	Reset Overflow and Set Word Length to 3
0B	RO4	Reset Overflow and Set Word Length to 4
0C	SO1	Set Overflow and Set Word Length to 1
0D	SO2	Set Overflow and Set Word Length to 2
0E	SO3	Set Overflow and Set Word Length to 3
0F	SO4	Set Overflow and Set Word Length to 4
34	NOP	No Operation

Conditional Jump

10	JOV	Jump if Overflow Set
11	JAZ	Jump if A Equal to Zero
12	JBZ	Jump if B Equal to Zero
13	JXZ	Jump if X Equal to Zero
14	JAN	Jump if A Negative
15	JXN	Jump if X Negative
16	JAB	Jump if A Equals B
17	JAX	Jump if A Equals X
18	NOV	Jump if Overflow not Set
19	NAZ	Jump if A not Equal to Zero
1A	NBZ	Jump if B not Equal to Zero
1B	NXZ	Jump if X not Equal to Zero
1C	NAN	Jump if A not Negative
1D	NXN	Jump if X not Negative
1E	NAB	Jump if A not Equal to B
1F	NAX	Jump if A not Equal to X

Shift

20	LLA	Logical Left A
21	LLB	Logical Left B
22	LLL	Logical Left Long
24	LRA	Logical Right A
25	LRB	Logical Right B
26	LRL	Logical Right Long
28	ALA	Arithmetic Left A
29	ALB	Arithmetic Left B
2A	ALL	Arithmetic Left Long
2C	ARA	Arithmetic Right A
2D	ARB	Arithmetic Right B
2E	ARL	Arithmetic Right Long

Operation Code	Mnemonic	Instruction Name
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Input/Output

30	IBS	Input Byte Serially
31	IBA	Input Byte to A
32	IBB	Input Byte to B
33	IBM	Input Byte to Memory
38	OBS	Output Byte Serially
39	OBA	Output Byte from A
3A	OBB	Output Byte from B
3B	OBM	Output Byte from Memory

Register Operate

40	ORA	OR B with A
41	XRA	Exclusive — OR B with A
42	ORB	OR A with B
43	XRB	Exclusive — OR A with B
44	INX	Increment X
45	DCX	Decrement X
46	AWX	Add Word Length to X
47	SWX	Subtract Word Length from X
48	INA	Increment A
49	INB	Increment B
4A	OCA	One's Complement A
4B	OCB	One's Complement B
4C	TAX	Transfer A to X
4D	TBX	Transfer B to X
4E	TXA	Transfer X to A
4F	TXB	Transfer X to B

Memory Reference

60	JMP	Jump
68	RTJ	Return Jump
70	IWM	Increment Word in Memory
78	DWM	Decrement Word in Memory
80	LDX	Load X
88	STX	Store X
90	MUL	Multiply
98	DIV	Divide
A0	ADA	Add to A
A8	ADV	Add Variable
B0	SBA	Subtract from A
B8	SBV	Subtract Variable
C0	CPA	Compare A
C8	CPV	Compare Variable
D0	ANA	And
D8	ANV	And Variable
E0	LDA	Load A
E8	LDV	Load Variable
F0	STA	Store A
F8	STV	Store Variable

Micro 800 and 810

Standard Options

	Part No.	Description	
Central Processor Option Boards	8401	Power Fail and Automatic Restart.	Provides interrupt when loss of power is imminent and when power is turned on.
	8402	Memory Parity.	Includes the memory parity generator and checker logic and an interrupt when an error is detected.
	8403	Memory Protection and Boundary Error.	Allows for a memory write protection on a block basis.
	8404	Real Time Clock.	Provides an internal interrupt at a crystal controlled timing rate.
	8405	Spare Memory Bit Control.	Provides a spare memory bit by expanding the memory byte length and I/O bus to 9 bits.
	8400	Option Board	Includes all of the above processor option items.
Utility Interfaces	8700	Input/Output Line Driver and Receiver Board.	Expands the internal I/O bus to an external bus allowing integration of up to 10 peripheral interfaces under program control, or concurrent data transfer with interrupt.
	8701	Parallel Teletype Controller	Assembles and disassembles serial information to and from the teletype for parallel transfer to and from the computer under program control or concurrent block transfer.
	8702	General Purpose I/O Board — Wire Wrap	Accommodates 14, 16, or 24 pin integrated circuit sockets in the following quantities: 135 units — 14 or 16 pin sockets 24 units — 24 pin sockets
	8703	Priority Interrupt Board	Allows interfacing of 8 external interrupt lines with expansion capability to 64 lines using 8 boards. Priority, timing, storage of interrupt, address generator functions and independent enabling or disabling of each interrupt are provided.
	8704	Direct Memory Access Selector Channel	Provides for transfer of 8 bit bytes directly between external devices and core memory. Transfer is in single block form or continuous cycling of one or linked blocks. An internal interrupt indicates "end of transfer" to the CPU program.

	Part No.	Description	
	8705	Input/Output Expander — Full Word (32 Bits)	Expands the 8 bit I/O bus into multiple (4) byte I/O under processor control. The outputs are independently latched. Outputs and inputs are standard DTL or TTL logic levels with the capability to interface with MUX-ADC's, DAC's, keyboards, and low speed peripheral devices such as incremental tape units, buffered line printers, and X-Y plotters.
Communications Options	8801	Synchronous Modem Controller	An interface to a 201 or equivalent data set, this option operates with point to point, or switched networks with optional automatic calling-answering for either 2-wire or 4-wire service. Data transfers are on a byte basis under concurrent Input/output or programmed control. A sync character detection circuit is provided in the interface for obtaining character synchronization. Interface levels are per EIA Standard RS-232-B.
	8803	Multiple, Low-Speed Modem Interface	This interface is designed to accommodate up to sixteen 103 type modems. It provides for two output circuits and four input circuits to each modem. Identical signals for all eight modems are transferred in parallel via the computer's byte I/O bus. All interface circuits comply with EIA RS-232-B standards.
	8804	Multiple, Teletype Interface	This interface board can accommodate up to 24 locally connected teletypes. Operation is 4-wire full duplex with 20 ma currents (60 ma is available as an option). Data for one of the 3 groups of eight teletypes is transferred in parallel via the byte I/O bus.
Device Interfaces	8907	Card Reader	Provides control of an 80 column card reader, 12 lines per column in hollerith or two binary bytes. Uses the Mohawk Data Sciences Corp. SCCR 6002, or equivalent. Code Conversion to BCD or binary is selectable under program control and data transfer can be on a character or on block basis with card reading rates of 225 or 400 cards per minute.
	8908	Paper Tape Reader/Punch	Consists of two separate functions which can be mounted on the same board. Data transfer is either a single word or concurrent block transfer with end of block interrupts provided. The punch data is buffered.
Special Interfaces			Numerous special interfaces of options can be provided by Micro Systems Inc. with relatively short lead times. These include I/O device controller interfaces such as alpha numeric CRT; rotating memory; magnetic tape unit, and MUX/ADC.

8001 Basic CPU

Memory Expander
 8704 DMA Channel Option
 8208 4K Core Memory
 8704 DMA Channel Option
 8208 4K Core Memory
 8704 DMA Channel Option
 8208 4K Core Memory
 8219 1K Core Option
 8208 4K Core Memory
 8219 1K Core Option

8500 Standard
 Basic Control Panel
 8501
 System Control Panel
 8502
 Operator Control Panel

8633 ASR-33TY



Power Supply

System Interface 4
 System Interface 3
 System Interface 2
 System Interface 1
 ROS 256 Words 4
 ROS 256 Words 3
 ROS 256 Words 2
 ROS 256 Words 1
 8304 Diagnostic ROS Option
 8400 Processor Options
 8000-2 Data Board
 8000-1 Control Board
 8000-2 Data Board

8003 Expansion Chassis

Memory Terminator
 8208 Core Memory
 8208 Core Memory
 8208 Core Memory
 8208 Core Memory



Utility

8700 IO Bus
Line Driver
 8701 Parallel TTY
 8702 General
Purpose I/O
 8703 Priority Interrupt
 8705 Input/Output
Exp. 32 x 32

System Interfaces

Communications

8801 Synchronous
Modem
 8803 Multiple, Low-Speed
Modem Interface
 8804 Multiple
Teletype Interface

Special Device Controllers

8901 Mag Tape Unit
 8902 Rotating Memory
 8903 Alpha Numeric CRT
 8905 MUX/ADC
 8907 Card Reader
 8908 Paper Tape
Reader/Punch

System Interface 11

System Interface 10

System Interface 9

System Interface 8

System Interface 7

System Interface 6

System Interface 5

I/O Expansion Terminator

Power Supply



MicroSystems



MicroSystems Inc.
A subsidiary of
Microdata Corporation

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Time-sharing traffic cop

Minicomputer can do concentration, pre-processing;
will handle communications for 96-terminal system

Suppose you have to process data coming into a central point from up to 96 terminals—including teletypewriter, and low- and medium-speed asynchronous modems and binary devices—and being transmitted at up to six different baud-rate combinations simultaneously. You can program a general-purpose computer to do the job, but you might be tying up an expensive machine for this data-communications task.

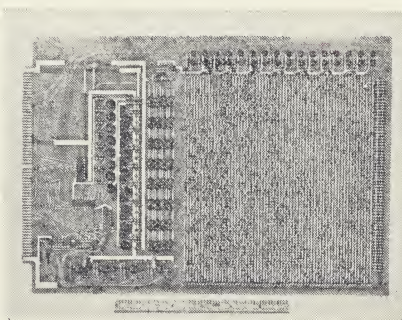
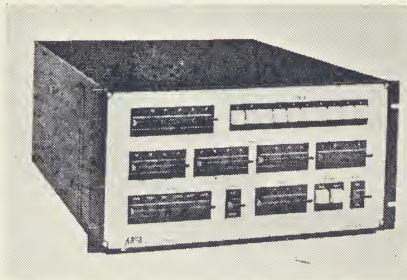
To avoid the need for costly tie-ups of this kind, data-processing system designers are developing special machines to handle communications [*Electronics*, March 31, p. 154].

At the Fall Joint Computer Conference, Nov. 18-20 in Las Vegas, Micro Systems Inc. will introduce its entry, the Micro 812.

William Roberts, MSI's vice president for research and engineering, says a typical application of the microprogrammed Micro 812 might be in a time-sharing system in which data from a number of lines is to be concentrated down to one phone line. "But we're not selling a concentrator," Roberts stresses. "We're selling a computer that can do concentration." MSI is aiming the machine at original equipment manufacturers for use as an interface unit to do data concentration, or as a pre-processor for larger computers "to free the larger computer from data communications worries," as Roberts puts it.

Not many machines like the Micro 812 are available, says Roberts. Interdata is the only other firm that he knows of offering a microprogrammed minicomputer specifically for data communications applications, and that machine can't handle as many input devices as MSI's can.

Stored program. A microprogrammed computer's control unit



Microprogrammed. Memory card, bottom photo, carries diodes that perform microprogramming in the 812. Diodes take up right half of card.

holds a stored program, while a fixed control machine is hard-wired. The program in the control unit can be quickly changed from one application to another, and tailors the computer for a given job without changing the hardware implementation. In the Micro 812, MSI officials say, 16 powerful microcommands are available to optimize the machine for the data-communications job, with microcommand word lengths of 16 bits. In effect, microprogramming in the machine simplifies most input/output interface requirements because the data from the teletypewriters or modems is timed and buffered internally without additional hardware or software.

In the Micro 812, the microprogram is contained in a discrete diode read-only memory with a 220-nanosecond cycle time. The basic

... first unit handles
inventory system ...

machine, which includes a 4,096-word by 9-bit core memory for the user's program, sells for \$10,000. Each group of 24 input lines dictates a need for an additional interface board in the computer. Besides handling the 96 low-speed teletypewriters (up to 360 bauds), the machine can be arranged to accommodate a maximum of 32 medium-speed input lines (less than 9,600 bauds). Each interface board will permit the computer to handle 24 additional teletypewriters or 16 additional modems.

Reserve. Roberts says a small computer without microprogramming would have half its I/O capability consumed in handling 16 teletypewriters; by contrast, the Micro 812 can accommodate its maximum 96 lines and mixed baud (bits per second) rates—110 bauds, 134.5 bauds, and 150 bauds, for example—using only 70% of its I/O capability.

In performing the I/O function of the teletypewriters, the microprogrammed read-only memory samples the inputs, reconstructs the characters it "sees" on a given input line, and, in a time-sharing system, may store a line of data—a printed line—before sending it to the central processor. Besides the microprogrammed processor and core memory, the basic machine includes a systems control panel, power supply, power-fail-automatic restart, memory parity, a real-time clock, six communications rate clocks, and provisions for additional communications interface boards. The unit is 8¾ by 17¾ by 23 inches.

The first Micro 812 machine went this month to Rydacom, a subsidiary of Ryder Systems Inc. of Miami, Fla., for use in an on-line warehouse inventory control system. MSI's Roberts expects the Micro 812 to account for some 30% of his firm's business next year; since introducing the Micro 800 and Micro 810 early this year, MSI has booked \$3 million worth of business from those two machines.

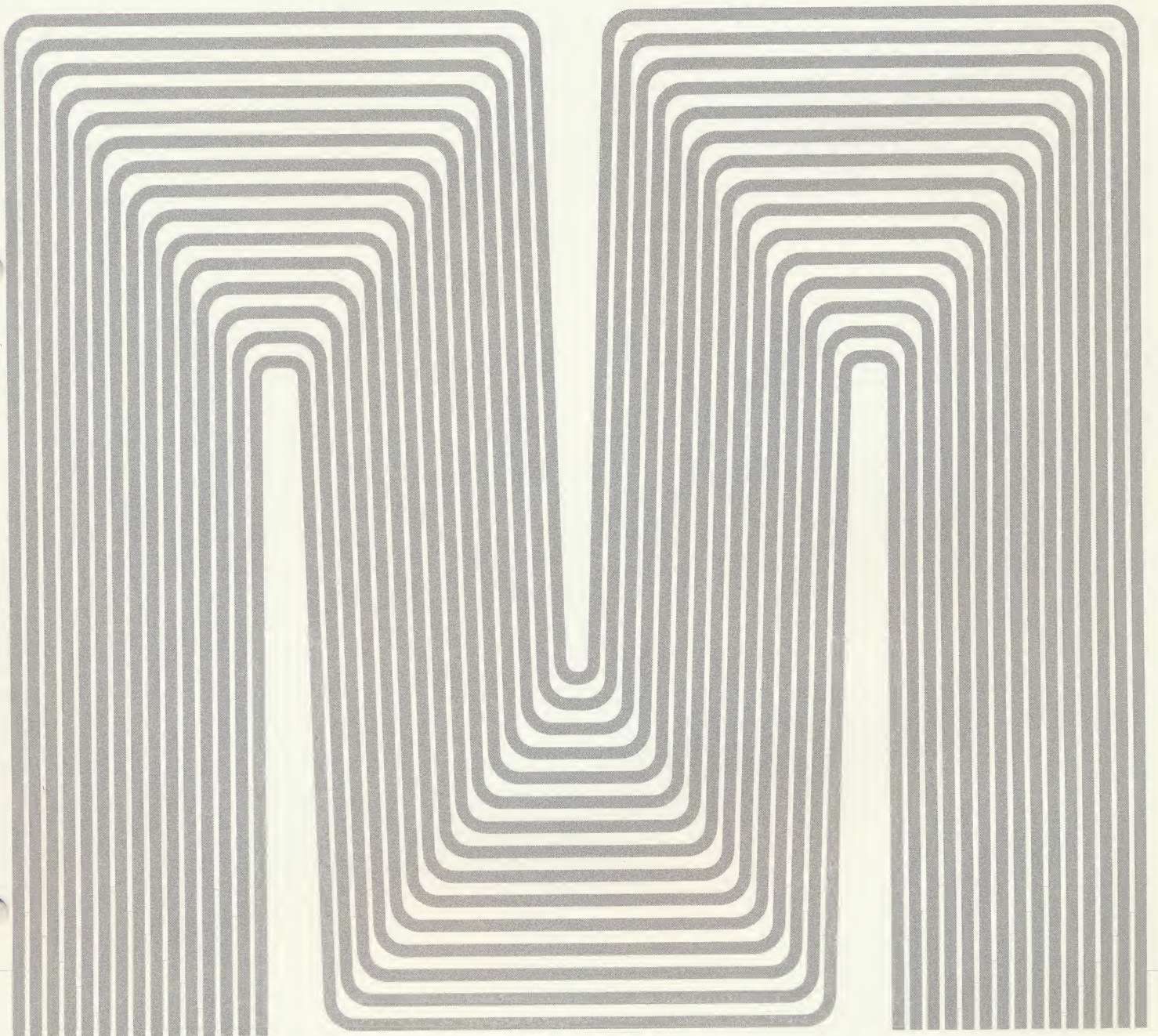
Typical delivery time for the Micro 812 will be 60 days.

Micro Systems Inc., 644 East Young St., Santa Ana, Calif. 92705 [340]

MicroSystems Inc.

**Micro 812
Communications Processor**

**Preliminary
Specifications**



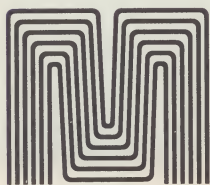
PRELIMINARY SPECIFICATIONS

MICRO 812

PROGRAMMABLE DATA

COMMUNICATIONS PROCESSOR

April 1970



Micro Systems Inc.
644 East Young Street
Santa Ana, California 92605

A Microdata Subsidiary



THE MICRO 812

PROGRAMMABLE DATA COMMUNICATIONS PROCESSOR

GENERAL FEATURES

The MICRO 812 is the third in a series of microprogrammed, low cost digital computers developed by Micro Systems and is specifically designed for data communications functions. It combines a powerful general purpose and communications oriented instruction set with numerous additional features which make it a versatile and outstanding price/performance data communications building block.

Key 812 features are:

- Handles up to 32 low speed asynchronous communications lines.
- Can accommodate four baud rates on communications lines.
- Handles mixed configurations of low speed asynchronous and synchronous devices.
- Has 105 general purpose and communications oriented instructions.
- Powerful string manipulation instructions.
- Variable precision operations.
- Memory byte addressability to 32K with supplementary magnetic bulk storage capability available.
- Pushdown stack for interrupts and recursive subroutines.
- Standard system includes real time clock, power fail interrupt, and automatic restart.
- Field proven design and software.
- Low system cost and excellent price/performance capability through microprogrammed control techniques.

APPLICATIONS

The Micro 812 is a field proven system, in volume production, which utilizes efficient microprogrammed firmware control to significantly reduce communications line costs in several major application areas.

As a stand-alone, interactive processing system, The MICRO 812 can be used as a central processor capable of handling up to 32 asynchronous lines, utilizing up to 32K bytes of core memory, and with the capability of handling supplemental magnetic disk storage of up to 256K bytes.

As a **data concentrator**, the MICRO 812 concentrates up to 32 low speed lines into a higher speed communications line linked to a large-scale computer. In this application, the 812 may be programmed to establish communication protocol, to perform code conversion, and to re-format data in order to reduce the communications burden on the main computer.

As a **pre-processor** for time sharing and information systems networks, the MICRO 812 provides an interface between a large-scale computer and a variety of low and medium speed communications lines. The MICRO 812 can be programmed to character edit, error check, and control or break character search.

As a **remote concentrator/batch terminal processing system**, the MICRO 812 can be combined with a modem and interfaced to a communications line connected to a pre-processor or directly linked to a large-scale central computer. In this application, the MICRO 812 can handle remote processing at the local site as well as time share off of a central computing system for large-scale processing.

CAPABILITIES

The MICRO 812 offers a variety of characteristics which previously have not been available in a low-cost, data communications system.

Compact, Modular Design

The basic MICRO 812 configuration (8-3/4" high, 17-3/4" wide and 23" deep) includes a microprogrammed processor, power supply, 4,096 X 8 bit core memory (1.1 microseconds cycle time), 1,026 words of read only store, power-fail automatic restart, and real time clock.

Up to 16,384 bytes of core memory and five communications and peripheral interface option boards can be added. An expansion chassis accommodates an additional 16K bytes of core memory and eight additional interface option boards. Supplemental magnetic storage can be supplied up to 256K bytes.

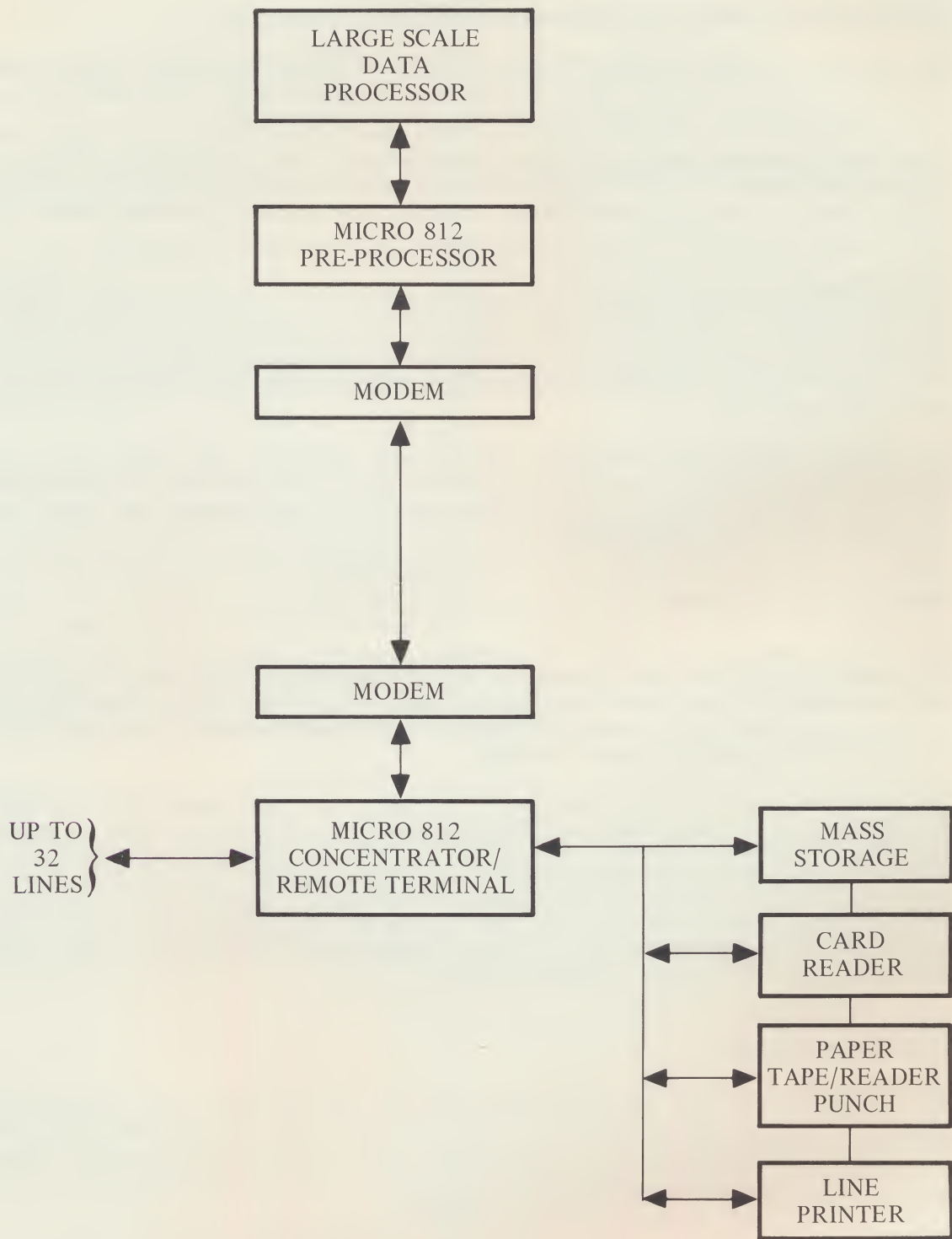
Multiple Rate Flexibility

A unique feature of the MICRO 812 is its ability to handle up to 32 low speed asynchronous communication lines with the character assembly and disassembly performed by the micro-programmed control of the processor. This is extremely efficient and results in lower communication line costs.

The system can handle mixed configurations of: low speed asynchronous modems (103 type), medium speed synchronous modems (201 type), serial teletypes (ASR 32, 33, 35, or 37) typewriters (IBM selectric), and serial binary devices.

Each group of eight lines can accommodate any signalling rate up to 300 baud in any one of the following code formats:

- 11 unit code (2 unit stop)
- 10 unit code (1 unit stop)
- 9 unit code (1 unit stop)
- 7.5 unit code (1.5 unit stop)



TYPICAL MICRO 812 COMMUNICATIONS SYSTEM

Powerful General Purpose and Communications Oriented Instructions

The MICRO 812 has a complete general purpose instruction set (which includes most MICRO 810 commands) plus many powerful communication device instructions such as cyclic code generation, ASCII parity generation, and character search.

Cyclic code generating instruction causes a 16-bit cyclic code to be generated in the A register for a block of memory starting with the address contained in the X register and ending with the address contained in the B register. This type of cyclic redundancy code (CRC) is used with the IBM Binary Synchronous Communications (BSC) systems.

Search Character instruction compares the bytes in the block of memory starting with the address contained in the X register and ending with the address contained in the B register with the bytes of a control list. When a match is found a jump is made to the address contained in the word following the matched byte in the control list. If the jump is made, the X register contains the address of the byte in the data block which compared with the byte in the control list.

The Generate ASCII Parity instruction generates and attaches an odd parity bit to each character and generates an 8-bit block longitudinal parity in the lower byte of the A register for all the characters starting with the address contained in the X register and ending with the address contained in the B register.

Pushdown Stack Capability

A pushdown stack is used to allow for re-entrant subroutine coding and for fast interrupt processing. The pushdown stack is a reserved area of memory (stack) into which registers are pushed (stored) and from which registers are pulled (loaded) on a last-in, first-out basis. Instructions are provided for pushing and pulling the A, B and X registers individually for all the MICRO 812 operational registers together.

The pushdown stack has a maximum size of 255 bytes and is fully contained in any single 256 page of core memory. Stack control is performed by a stack pointer word containing the address of the last used byte at the top of the stack. It is decremented as each byte is pushed into the stack and is incremented as each byte is pulled from the stack. When a register or group of registers is to be pushed into the stack, a check is made to see if the registers can be stored without causing the stack to fill the memory page. If there is not sufficient storage available, the stack pointer is unaltered and a return jump is made to the address contained in the stack overflow pointer.

Field Proven Software

The MICRO 812 software has been derived from the MICRO 810 General Purpose Mini Computer which has been produced in volume since early 1969. This provides the MICRO 812 with a complete, field proven software library which includes a cross assembler written in FORTRAN IV (AP812), two-pass assembler (MAP812), teletype operating system (TOS), symbolic tape editor (TED), and diagnostic programs.

MICRO 812

COMMUNICATIONS I/O FUNCTIONAL DESCRIPTION

The unique input/output performance features of the MICRO 812 are accomplished through the use of a high speed firmware program. Entry to the communications firmware routine is accomplished automatically through the use of an internal interrupt generated by one or more of four independent communication rate clocks.

Since the input devices are all asynchronous, they are sampled at a multiple of the baud rate (five times) to perform an async-to-sync conversion. This multiple rate sampling is used to detect the leading edge of the start element and minimizes the uncertainty by sampling each signalling element at or near its center. Once this is detected, each of the signalling elements is sampled once and the character is automatically assembled in memory. On output, all lines are in bit phase, with the exception of the 7.5 unit code which is handled at twice the signalling rate.

Line Group

A line group consists of a set of eight lines having the same signalling rate and code and which are processed together. Interface circuitry for the eight lines is located on a single board which interfaces with the processor by means of the byte I/O facility. Data transfers between the interface board and the processor are parallel eight-bit bytes with bits of the byte corresponding to the eight individual lines of the line group.

Each group of eight lines requires a 64 byte area of memory for processing the eight inputs and eight outputs. These areas contain two byte controls for each input, four byte controls for each output, and four bytes of control for the group.

Queues

A 64 byte area of memory is used as an input queue for received characters. When a character is received on one of the lines, the line identification and the character are placed in the queue. A 64 byte area of memory is also used as an output queue. When a character is removed from the output buffer for transmission, the line identification is placed in the output queue. Appearance of a line identification in the output queue signifies that a new character may be placed in the corresponding output buffer.

MICRO 812 SPECIFICATIONS

TYPE

A byte oriented, software programmable, microprogrammed computer designed for communication system applications.

ARITHMETIC

Multi-precision, parallel, binary, fixed point, two's complement.

WORD LENGTH

Memory is byte addressable; registers are 16 bits in length; arithmetic operations are either fixed (16 bits) or variable (8, 16, 24, or 32 bits) in length.

REGISTERS

The Micro 812 has six operational registers:

A Register	16 bit Accumulator
B Register	16 bit Auxiliary Accumulator for low order 16 bits of 24 and 32 bit data
X Register	16 bit Index Register
P Register	15 bit Program Counter
W Register	2 bit word length register
O Register	1 bit overflow flag

INSTRUCTIONS

The MICRO 812 has 105 instructions and will execute all standard software of the MICRO 810.

ADDRESSING

Eight addressing modes including relative, index, indirect, literal and direct.

CORE MEMORY

Memory modules of 4,096 bytes by 8 bits. The memory operates at 1.1 microseconds full cycle time. Memory is expandable from 4,096 bytes to a maximum of 32,768 bytes. Memory parity is an option.

READ ONLY STORE

Read Only Storage (ROS) uses discrete diodes in printed circuit board modules of 256 16-bit words. 1024 words are used in the MICRO 812 communication processor. ROS cycle time is 220 nanoseconds. The ROS contains a bootstrap loader as well as all macro instructions and input/output firmware.

INPUT/OUTPUT

An 8-bit parallel I/O bus permits programmed transfers, fully automatic concurrent transfers, and automatic asynchronous line multiplexing. An optional Direct Memory Access (DMA) Channel provides a maximum transfer rate of 909,000 bytes per second.

COMMUNICATION INTERFACES

The MICRO 812 will accommodate up to 32 low speed lines (modem, teletype) and medium speed lines (201 modem, 202 modem or equivalent).

MIXED BAUD RATES

50 to 300 baud asynchronous variable size character codes using 5, 7 or 8 bits per character.

LINE DISTORTION

Input line distortions of up to $\pm 35\%$ can be accommodated with no degradation of performance: output line distortion is 3% maximum.

INTERRUPTS

A priority interrupt system allows internal interrupts on power failure, real time clock, memory parity error, communication rate clocks, and external interrupts on the byte I/O bus.

POWER FAIL

Power fail detection and automatic restart is provided as a standard feature.

REAL TIME CLOCK

A crystal oscillator derived, programmable real time clock is provided as a standard feature.

LOGIC

TTL logic elements including an extensive amount of MSI types, packaged in DIP ceramic packages are used. DTL circuitry is used for I/O interfaces.

CABINET

The processor, memory to 16K, 4 I/O interfaces, 1 DMA channel, power supply, and fan are enclosed in a cabinet measuring 8-3/4" high, 17-3/5" wide, and 23" deep. Fully expanded cabinet weight is 75 pounds. Additional I/O interfaces plus expansion up to 32K of memory can be obtained with a standard expansion cabinet.

PANEL

The basic control panel provides basic control switches. An optional system control panel permits display of all registers, manual microcommand execution, and computer control switches.

POWER

115/230VAC $\pm 10\%$, 47-63 cycles, 340 watts AC.

ENVIRONMENT

0-50°C (32° - 122°F), 10 - 90% humidity (without condensation).

MICRO 812 INSTRUCTIONS

Operation Code	Mnemonic	Instruction Name
Control		
00	HLT	Halt
01	TRP	Trap
02	ESW	Enter Sense Switches
03	EDR	Enable/Disable Rate Generator
04	DI $\bar{N}$	Disable Interrupt System
05	EIN	Enable Interrupt System
06	DRT	Disable Real Time Clock
07	ERT	Enable Real Time Clock
08	RO1	Reset Overflow and Set Word Length to 1
09	RO2	Reset Overflow and Set Word Length to 2
0A	RO3	Reset Overflow and Set Word Length to 3
0B	RO4	Reset Overflow and Set Word Length to 4
0C	SO1	Set Overflow and Set Word Length to 1
0D	SO2	Set Overflow and Set Word Length to 2
0E	SO3	Set Overflow and Set Word Length to 3
0F	SO4	Set Overflow and Set Word Length to 4
34	NOP	No Operation
Conditional Jump		
10	JOV	Jump if Overflow Set
11	JAZ	Jump if A Equal to Zero
12	JBZ	Jump if B Equal to Zero
13	JXZ	Jump if X Equal to Zero
14	JAN	Jump if A Negative
15	JXN	Jump if X Negative
16	JAB	Jump if A Equals B
17	JAX	Jump if A Equals X
18	NOV	Jump if Overflow not Set
19	NAZ	Jump if A not Equal to Zero
1A	NBZ	Jump if B not Equal to Zero
1B	NXZ	Jump if X not Equal to Zero
1C	NAN	Jump if A not Negative
1D	NXN	Jump if X not Negative
1E	NAB	Jump if A not Equal to B
1F	NAX	Jump if A not Equal to X

Operation Code	Mnemonic	Instruction Name
Shift		
20	LLA	Logical Left A
21	LLB	Logical Left B
22	LLL	Logical Left Long
24	LRA	Logical Right A
25	LRB	Logical Right B
26	LRL	Logical Right Long
28	ALA	Arithmetic Left A
29	ALB	Arithmetic Left B
2A	ALL	Arithmetic Left Long
2C	ARA	Arithmetic Right A
2D	ARB	Arithmetic Right B
2E	ARL	Arithmetic Right Long
Input/Output		
30	IBS	Input Byte Serially
31	IBA	Input Byte to A
32	IBB	Input Byte to B
33	IBM	Input Byte to Memory
38	OBS	Output Byte Serially
39	OBA	Output Byte from A
3A	OB B	Output Byte from B
3B	OB M	Output Byte from Memory
Register Operate		
40	ORA	OR B with A
41	XRA	Exclusive—OR B with A
42	ORB	OR A with B
43	XRB	Exclusive—OR A with B
44	INX	Increment X
45	DCX	Decrement X
46	AWX	Add Word Length to X
47	SWX	Subtract Word Length from X
48	INA	Increment A
49	INB	Increment B
4A	OCA	One's Complement A
4B	OCB	One's Complement B
4C	TAX	Transfer A to X
4D	TBX	Transfer B to X
4E	TXA	Transfer X to A
4F	TXB	Transfer X to B

Operation Code	Mnemonic	Instruction Name
Special Instructions		
50	RTN	Return
51	CAL	Call
52	PLX	Pull X
53	PSX	Push X
54	PLA	Pull A
55	PSA	Push A
56	PLB	Pull B
57	PSB	Push B
58	MST	Multiply Step
59	ADX	Add to X
5A	JEP	Jump Even Parity
5B	EBX	Exchange B and X
5C	MOV	Move
5D	GCC	Generate Cyclic Code
5E	SCH	Search
5F	GAP	Generate ASCII Parity
Memory Reference		
60	JMP	Jump
68	RTJ	Return Jump
70	IWM	Increment Word in Memory
78	DWM	Decrement Word in Memory
80	LDX	Load X
88	STX	Store X
90	LDB	Load B
98	STB	Store B
A0	ADA	Add to A
A8	ADV	Add Variable
B0	SBA	Subtract from A
B8	SBV	Subtract Variable
C0	CPA	Compare A (Less than, equal to, greater than.)
C8	CPV	Compare Variable (Less than, equal to, greater than.)
D0	ANA	And
D8	ANV	And Variable
E0	LDA	Load A
E8	LDV	Load Variable
F0	STA	Store A
F8	STV	Store Variable

MICRO 812 STANDARD OPTIONS

Communications Options

PART NO.	DESCRIPTION	
8801	Synchronous Modem Controller	An interface to a 201 or equivalent data set, this option operates with point to point, or switched networks with optional automatic calling-answering for either 2-wire or 4-wire service. Data transfers are on a byte basis under concurrent Input/Output or programmed control. A sync character detection circuit is provided in the interface for obtaining character synchronization. Interface levels are per EIA Standard RS-232B.
8803	Multiple, Low-Speed Modem Interface	This interface is designed to accomodate up to 8 103-type modems for exchange lines and 16 for point to point lines. It provides for two output circuits and four input circuits to each modem. Identical signals for all eight modems are transferred in parallel via the computer's byte I/O bus. All interface circuits comply with EIA Standard RS-232B.
8804	Multiple, Teletype Interface	This interface board can accommodate up to 24 locally connected teletypes. Operation is 4-wire full duplex with 20 ma currents (60 ma is available as an option). Data for one of the 3 groups of eight teletypes is transferred in parallel via the byte I/O bus.
8850	Teletype Converter	A 3-1/2" X 1-3/8" printed circuit board which converts one of the input/output connections of the 8804 asynchronous teletype interface board to an asynchronous modem line.
8851	Modem Converter	A 3-1/2" X 1-3/8" printed circuit board which converts one of the input/output connections of the 8803 asynchronous modem interface board to a teletype line.
8852	Communication Termination Assembly	A rack mounted termination panel with the capability of connection to 16 teletype or 16 point to point asynchronous modems.

Utility Interfaces

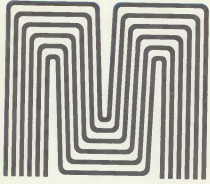
PART NO.	DESCRIPTION	
8700	Input/Output Line Driver and Receiver Board	Expands the internal I/O bus to an external bus allowing integration of up to 10 peripheral interfaces.
8701	Parallel Teletype Controller	Assembles and disassembles serial information to and from the teletype for parallel transfer to and from the computer under program control or concurrent block transfer.
8702	General Purpose I/O Board—Wire Wrap	Accommodates 14, 16, or 24 pin integrated circuit sockets in the following quantities: 135 units — 14 or 16 pin sockets 24 units — 24 pin sockets.
8703	Priority Interrupt Board	Allows interfacing of 8 external interrupt lines with expansion capability to 64 lines using 8 boards. Priority, timing, storage of interrupt, address generator functions and independent enabling or disabling of each interrupt are provided.
8704	Direct Memory Access Selector Channel	Provides for transfer of 8 bit bytes directly between external devices and core memory. Transfer is in single block form or continuous cycling of one or linked blocks. An internal interrupt indicates "end of transfer" to the CPU program.
8907	Card Reader Controller	Provides control of an 80 column Mohawk Data Sciences Corp. SCCR 6002, or equivalent card reader. Code conversion to 8 bit EBCDIC or 12 bit Hollerith is selectable under program control. Data transfers can be on a column or on a block basis with card reading rates of 225 or 400 cards per minute.
8908	Paper Tape Reader/Punch Controller	Consists of two separate interfaces which can be mounted on the same board. Data transfer is either a single byte or concurrent block transfer with end of block interrupts provided. The punch data is buffered.

8950 Rotating Memory
 System Controller

Interface board for control of IDS Models
7064, (256K 8-bit words; 2.1 million bits),
7032 (128K 8-bit words; 1.2 million bits),
and 7008 (32K 8-bit words; 0.3 million bits).

Special Interfaces

Numerous special interface controllers can be provided by Micro Systems with relatively short lead times. These include I/O device controller interfaces such as alpha numeric CRT; X-Y CRT, MUX/ADC, and magnetic tape.



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